AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An imaging device, comprising:

a pixel array circuit that outputs an image signal including ~~and~~ a background signal caused by at least one of non-uniformity of illumination and optical shading;

a memory array circuit, coupled to said pixel array circuit, ~~said memory array circuit~~ to store the background signal ~~configurable to store an output from said pixel array~~; and

a data subtraction circuit, coupled to said memory array circuit and said pixel array circuit, said data subtraction circuit performing a data subtraction operation on the pixel array output to remove said background signal from said image signal.

2. (Original) The imaging device according to claim 1, wherein the imaging device further comprises an image enhancement circuit that performs an edge enhancement operation on the image signal received from the data subtraction circuit.

3. (Currently Amended) The imaging device according to claim 2, wherein the imaging device further comprises an analog-to-digital converter, which converts the signal received from the image enhancement circuit to a digital signal.

4. (Original) The imaging device according to claim 1, wherein each memory element in said memory array corresponds to a pixel circuit in said pixel array circuit.

5. (Cancelled)

6. (Currently Amended) A method for processing analog image data in an imager chip, said method comprising the steps of:

receiving analog image data, said analog image data including a background signal, caused by at least one of non-uniformity of illumination and optical shading, and a temporal signal;

performing a subtraction operation to separate the background signal from the temporal signal; and

performing an enhancement operation on the temporal signal to generate an edge-enhanced signal.

7. (Original) The method according to claim 6, wherein the analog image data is received from a pixel array in said imager chip.

8. (Original) The method according to claim 6, wherein said analog image data is received from a memory array in said imager chip.

9. (Original) The method according to claim 6, wherein the background signal comprises an offset variation signal.

10. (Currently Amended) The method according to claim 6, wherein the background signal further comprises a fixed pattern noise signal.

11. (Original) The method according to claim 6, further comprising the step of performing an analog-to-digital conversion to the edge-enhanced signal in said imager chip.

12. - 50. (Cancelled)

51. (Currently Amended) A memory circuit comprising:

an input lead for receiving at least one [[a]] readout signal from a pixel ~~circuit~~ array comprising at least a background signal;

a first capacitive element connected to the input lead, the first capacitive element storing a voltage indicating a level of ~~a~~ the background signal ~~received readout signal~~;

a second capacitive element;

a switching element connected between the first and second capacitive elements and, when switched on, providing a conductive path through which a previous voltage stored by the second capacitive element is combined with the stored voltage from the first capacitive element to form a combined signal; and

a readout element connected to provide a readout signal from the first capacitive element when the switching element is switched off and from the first and second capacitive elements when the switching element is switched on,

wherein the combined signal is a signal to be subtracted from an image signal.

52. (Currently Amended) An imaging ~~processing~~ system, comprising:

~~a memory unit;~~

~~a processing circuit coupled to said memory unit, said processing circuit comprising:~~

a pixel array circuit for outputting ~~that outputs~~ an image signal ~~and~~ including a background only signal;

a memory array circuit, coupled to said pixel array circuit, for receiving and storing the background only signal ~~said memory array circuit configurable to store an output from said pixel array~~; and

a data subtraction circuit, coupled to said memory array circuit and said pixel array circuit~~, said data subtraction circuit~~ for performing a data subtraction ~~operation on the pixel array output~~ to remove said background only signal from said image signal using said stored background signal.

53. (Currently Amended) The imaging ~~processing~~ system according to claim 52, ~~wherein the processing system~~ further ~~comprises~~ comprising an image enhancement circuit that performs an edge enhancement operation on the image signal received from the data subtraction circuit.

54. (Currently Amended) The imaging ~~processing~~ system according to claim 53, ~~wherein the processing system~~ further ~~comprises~~ comprising an analog-to-digital converter, which converts the output signal from the image enhancement circuit.

55. (Currently Amended) The imaging ~~processing~~ according to claim 52, wherein each memory element in said memory array corresponds to a pixel circuit in said pixel array circuit.

56. (Cancelled)

57. (Currently Amended) An integrated circuit, comprising:

a substrate;

a pixel array circuit, formed in said substrate, for providing an image signal and a background signal caused by at least one of non-uniformity of illumination and optical shading;

a memory array circuit, formed in said substrate, coupled to said pixel array circuit, each memory element in said memory array corresponds to a pixel circuit in said pixel array circuit, for storing ~~said image signal and~~ the background signal; and

a data subtraction circuit, formed in said substrate, coupled to said memory array circuit and said pixel array circuit, ~~said data subtraction circuit~~ for performing a data subtraction ~~operation~~ to remove said background signal from said image signal using said stored background signal.

58. (Original) The integrated circuit according to claim 57, wherein the integrated circuit further comprises an image enhancement circuit that performs an edge enhancement operation on the image signal received from the data subtraction circuit.

59. (Original) The integrated circuit according to claim 58, wherein the integrated circuit further comprises an analog-to-digital converter, which converts the signal output from the image enhancement circuit.

60. (Cancelled)

61. (Cancelled)

62. (New) The imaging device according to claim 1, wherein the background signal further comprises a fixed pattern noise signal.

63. (New) The imaging device according to claim 1, wherein the background signal is readout from a no-data area of a memory disk.

64. (New) The integrated circuit according to claim 52, wherein the background only signal is readout from a no-data area of a memory disk.

65. (New) The integrated circuit according to claim 52, wherein the background only signal further comprises a fixed pattern noise signal.

66. (New) The integrated circuit according to claim 57, wherein the background signal further comprises a fixed pattern noise signal.